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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. **A-382WOC**

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

and invented by:

Kouichi IKEDA et al

If a **CONTINUATION APPLICATION,** *check appropriate box and supply the requisite information:*

☒ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **PCT/JP99/02564 and PCT/JP99/02565**

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Enclosed are:

Application Elements

1. ☐ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **16 (sixteen)** pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

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Docket No. A-382WOC
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets **5 (five)**
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
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   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
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UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. A-382WOC
	Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below):*

Inventor Information Sheet (Patent Bibliographical Data)

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

UTILITY PATENT APPLICATION TRANSMITTAL
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(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. A-382WOC
Total Pages in this Submission

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	10	- 20 =	0	x	$18.00	$0.00
Indep. Claims	4	- 3 =	1	x	$80.00	$80.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$790.00

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Dated: **November 17, 2000**

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Koulchi IKEDA et al**			Docket No. **A-382WOC**
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Invention: **SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME**

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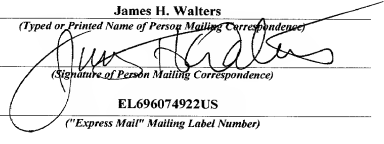

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APPLICATION INFORMATION

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Title Line Two:: FACTURING THE SAME
Total Drawing Sheets:: 5
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: A-382WOC
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 802
Registration Number One:: 35731

CONTINUITY INFORMATION

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> Application One:: PCT/JP99/02564
Filing Date:: 05-18-1999

This application is a:: CONTINUATION OF
> Application Two:: PCT/JP99/02565
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PRIOR FOREIGN APPLICATIONS

Foreign Application One:: 10-153818
Filing Date:: 05-19-1998
Country:: JAPAN
Priority Claimed:: Yes
Foreign Application Two:: 10-153819
Filing Date:: 05-19-1998
Country:: JAPAN
Priority Claimed:: Yes

Source:: PrintEFS Version 1.0.1

SPECIFICATION

Semiconductor Device and Method For Manufacturing the Same

Technical Field

The invention relates to a semiconductor device mounted on a memory substrate, a mother board, or the like and a method for manufacturing the same.

Background Art

A semiconductor chip such as a memory chip cutout from a semiconductor wafer is generally mounted on a printed substrate or the like in a packaging condition. However, an outer size of a package is considerably larger than the size of a various types of the semiconductor chips themselves and therefore, there is a certain limit in the number of the packages mountable on the printed substrate or the like.

On the other hand, recently, a multichip module (MCM), in which a plurality of semiconductor chips are mounted on the substrate, is being popularized. Using the multichip module allows the followings: (1) miniaturization of a mounting area and weight reduction accompanying with this, (2) realization of a high performance and high speed by high density wiring and bear chip mounting, and (3) keeping high reliability.

By the way, in the multichip module capable of a high density mounting described above, a plurality of semiconductor chips are mounted on a single substrate and therefore, a defect

ratio of respective semiconductor chips is accumulated to make a total defect ratio of the module large. For example, in the case where four memory chips are implemented on a single module substrate, only one defect memory chip causes overall defect of the module. Therefore, it is necessary handling to replace the defect memory chip as a repairing work and discard the overall module as a defect product. Thus, a low yield and a low efficiency occur. In addition, in the case where a plurality of semiconductor chips are mounted on a single substrate, each one of respective chips is mounted on a single substrate to complicate a manufacturing process.

Disclosure of the Invention

The present invention is achieved in consideration of such points and an object thereof is to provide a semiconductor device and a method for manufacturing thereof capable of reducing a defect ratio in manufacturing the semiconductor device mountable with high density and capable of simplifying the process.

In the present invention, after a plurality of identical semiconductor chips (preferably, memory chip) are formed on the semiconductor wafer or after wiring, resin sealing, and terminal formation is carried out for these semiconductor chips, a go/no-go test (quality test) is conducted for each semiconductor chip. According to the result, a unit of one or a plurality of semiconductor chips is divided to form the semiconductor device. Dividing semiconductor chips is carried out according to the result of quality test. When

the semiconductor device comprising a plurality of semiconductor chips is manufactured, some defective semiconductor chips among them does not cause defect of overall semiconductor device. Thus, the defect rate in manufacturing the semiconductor device can be reduced. Because the semiconductor device comprising a plurality of semiconductor chips can be used in a process thereafter and thus, in comparison with application of combination of a plurality of semiconductor devices comprising a single semiconductor chip, the process thereafter can be simplified.

Particularly, by practice of a mounting step composed of wiring, resin sealing, and terminal formation for respective semiconductor chips formed on the semiconductor wafer, in comparison with the case where the mounting step is carried out after respective semiconductor chips are individually divided more simplification of the process become possible.

It is preferable that semiconductor chips, particularly memory chips, according to the result of quality test are divided in every group made of four pieces if four is possible to handle, every two pieces if four is impossible but two are possible to handle, and every one piece if two are impossible to handle. As described above, priority of dividing in a group of a plurality of pieces makes efficient manufacture of the semiconductor device of the large (for four pieces) unit possible.

Brief Description of the Drawings

FIG.s 1A to 1D are diagrams showing a manufacturing process of a memory module of a first embodiment;

FIG. 2 is a diagram showing an outline of a memory chip formed on a semiconductor wafer;

FIG.s 3A and 3B are diagrams showing an example of dividing method for the memory chip formed on the semiconductor wafer;

FIG.s 4A to 4D are diagrams showing the manufacturing process of the memory module of a second embodiment;

FIG. 5 is an enlarged sectional view of the memory chip mounted by CSP; and

FIG. 6 is a diagram showing a connecting status between respective memory chips connected each other.

Best Mode for Carrying Out the Invention

A memory module of a first embodiment according to the present invention will be described below with reference to drawings. FIG.s 1A to 1D are diagrams showing a manufacturing process of a memory module of a first embodiment.

First, as shown in FIG.s 1A and 1B, a semiconductor wafer 2 which is, for example, a flake of silicon monocrystal, is introduced to form identical memory chips 1 thereon (a first step). Respective regions surrounded by a dotted line in FIG. 1B shows one unit of the memory chip 1 (the smallest unit of division) and on the semiconductor wafer 2, a plurality of the memory chips 1 are formed.

FIG. 2 is a diagram showing an outline of the memory chip 1 formed on the semiconductor wafer 2. As shown in FIG. 2, the memory chip 1 is configured by including the semiconductor

wafer 2 with a predetermined size and a plurality of chip pad (pad for the chip) s 3 formed on the surface of the semiconductor wafer 2. The chip pad 3 is a connecting terminal to carry out an electric connection to the substrate on which the memory chip 1 is mounted.

In a status in which a plurality of memory chips 1 have been formed on the semiconductor wafer 2 in such manner, then each of memory chips 1 is subjected to quality test (a second step). For example, to the chip pad 3 formed on each memory chip 1, a test probe is pressed to be electrically contacted for carrying out various function tests. By carrying out the quality test of each memory chip 1 for a unit of a whole the semiconductor wafer 2, in other words, by the quality test of a plurality of memory chips 1 formed on the semiconductor wafer 2 carried out at once, test efficiency is realized.

Next, on the basis of a result of the quality test in the second step, as shown in FIG. 1C, the memory chips 1 determined good are divided for the unit of a single or a plurality pieces (two or four pieces) (a third step).

FIG. s 3A and 3B are diagrams showing an example of dividing method for a plurality of memory chips 1 formed on the semiconductor wafer 2. FIG. 3A is a diagram showing the result of the quality test of each memory chip 1 in the second step as described above. Circled and crossing marks denote memory chips 1 determined good and memory chips 1 determined bad, respectively. FIG. 3B is a diagram showing how to divide memory chips 1 determined good in FIG. 3A. An area surrounded by a solid line shows a unit of dividing. As described above,

the memory chips 1 are divided in a unit of a group made of one or a plurality pieces (2 or 4 pieces). Preferably, dividing is carried out for a group made of pieces as many as possible. Therefore, the process according to the dividing method shown in FIG. 3B, four pieces are divided in the case where four memory chips 1 can be divided as a unit, two pieces are divided as a unit in the case where four memory chips 1 cannot be divided, and only one chip is divided in the case where two memory chips 1 cannot be divided. In the case where this method for dividing is applied to the result of quality test shown in FIG. 3A, as shown in FIG. 3B, 1 set produced by dividing for four memory chips 1 as a unit is taken out, 3 sets produced by dividing for two memory chips 1 as a unit is taken out, and 3 sets produced by dividing for one memory chips 1 is taken out. According to such manner, the semiconductor device comprising one or a plurality of memory chips is fabricated.

Next, as shown in FIG. 1D, the memory chips 1 which are divided are mounted on the substrate 4 to complete finally a memory module 10a made by getting four pieces of the memory chips 1 as one unit, memory module 10b made by getting two pieces of the memory chips 1 as one unit, or memory module 10c made by getting one pieces of the memory chips 1 (a fourth step). For example, as a method of mounting on the substrate 4, the chip pad 3, which is formed on the memory chip 1, is connected to an electrode (not illustrated) formed on the substrate 4 by using a bonding wire.

When bit configuration of respective memory chips 1 is 16 M × 4 bits, for example, the memory module 10a containing

four memory chips 1 can be used as memory device of any one of 16 M × 16 bits, 32 M × 8 bits, and 64 M × 4 bits according to wiring manner on the substrate (not illustrated) on which the memory module 10a is implemented. In addition, the memory module 10a can be handled as same as a single memory device. Therefore, processes of implementing on other substrates can be simplified.

Similarly, when bit configuration of respective memory chips 1 is 16 M × 4 bits, the memory module 10b containing two memory chips 1 can be used as memory device of any one of 16 M × 8 bits and 32 M × 4 bits according to wiring manner on the substrate on which the memory module 10b is implemented. In addition, the memory module 10b can be handled as same as a single memory device. Therefore, processes of implementing on other substrates can be simplified and parts can be miniaturized.

As described above, manufacture of the memory module 10 is carried out by forming a plurality of identical memory chips on the semiconductor wafer 2 and dividing the memory chips 1 judged to be nondefective by quality test. Therefore, a defect part of memory chips 1 does not cause defect product of overall memory module 10 to allow reducing the defect rate in manufacture of the memory module 10.

Quality test of a plurality of memory chips 1, which is implemented on the semiconductor wafer 2, is simultaneously carried out in a unit of overall semiconductor wafer 2 as a single group. Therefore test efficiency can be improved. Furthermore, memory chips are divided in a unit of a group

made of one or a plurality of pieces (two or four pieces). Preferably, dividing is simultaneously carried out for a group made of pieces as many as possible. Namely, dividing for four pieces as a group as possible allows efficient manufacture of the memory module 10a for four pieces as a group.

Furthermore, the memory module 10a and the memory module 10b are mounted by the divided group of a plurality of memory chips 1 formed on the semiconductor wafer 2. In other words, a plurality of memory chips 1 are mounted in the status of connecting each other. Therefore, in comparison with the case where an individual memory chip 1 is divided from the semiconductor wafer 2 one by one to mount with a distance from each other memory chip 1 resulting in formation of the memory module, miniaturization of components can be realized by high density mounting. Also, mounting of a plurality of semiconductor chips 1 at once can be carried out and thus, fabrication process can be simplified.

Next, the memory module of a second embodiment by an application of the present invention will be subsequently described. The memory module according to the present embodiment is fabricated by a chip size package mounting technique (CSP). FIG.s 4A to 4D are diagrams showing the fabrication procedure of the memory module according to the present embodiment.

First, as shown in FIG.s 4A and 4B, the semiconductor wafer 12 is introduced to form identical memory chips 11 on this semiconductor wafer 12 (the first step). A plurality of respective regions surrounded with a dotted line in FIG.

4B show a single unit (the minimum unit of dividing) of the memory chip 11 after CSP mounting. Next, for a whole of the semiconductor wafer 12 in the status of forming a plurality of memory chips 11, as shown in FIG. 4C, after conducting wiring and resin sealing, CSP mounting is carried out to form the terminal (the second step).

FIG. 5 is an enlarged sectional view of the memory chip 11 mounted by CSP. As shown in FIG. 5, the memory chip 11 mounted by CSP is configured by including the semiconductor wafer 12, a wiring pattern 13, a via post 14, barrier metal 15, a resin layer 16, and a solder ball 17.

The wiring pattern 13 is formed by processing a metal thin film, which has been formed on a surface of the semiconductor wafer 12, by using a resist followed by electrolytic plating processing. The via post 14 is connected to the wiring pattern 13 and the barrier metal 15 is formed on top thereof. The resin layer 16 seals the surface of the semiconductor wafer 12. The resin layer 16 has a thickness almost equal to a height of the via post 14 and is formed to allow the barrier metal 15 to expose to outside in resin sealing. The solder ball 17 is a connection terminal to electrically connect the substrate for mounting of the memory chip 11.

In the status in which according to such a manner, a plurality of memory chips 11 formed on the semiconductor wafer 12 have been mounted by CSP, then quality test is conducted for respective memory chips 11 (the third step). For example, by pressing a test probe to the solder ball 17 formed corresponding to respective memory chips 11 to electrically

contact, various function tests are conducted. Quality test of the memory chip 11 is conducted for whole semiconductor wafer 12 as a unit, in other words, quality test of a plurality of memory chips 11 formed on the semiconductor wafer 12 is conducted at once and hence, efficiency of the test is improved.

Subsequently, on the basis of a result of quality test in the third step, as shown in FIG. 4D, memory chips 11, which have been mounted by CSP and determined as good, are divided in the unit of one or a plurality (two or four pieces) of semiconductor chips and then, finally, either the memory module 20a having four memory chips 11 divided, the memory module 20b having two memory chips 11 divided, or the memory module 20c having one memory chip 11 divided is completed (a fourth step). Concretely, the dividing method shown in FIG.s 3A and 3B applied to the first embodiment described above is adopted.

As described above, after forming a plurality of identical memory chips 11 on the semiconductor wafer 12, the CSP mounting is carried out. Among respective memory chips 11 mounted by CSP, those only determined as good by a quality test are divided to fabricate the memory module 20 as the semiconductor device and thus, it does not take place that a part of defective memory chips 11 contained in the memory module 20 makes whole of the memory module 20 defective. Therefore, defect ratio can be reduced in fabrication of the memory module 20.

For the memory module 20a and memory module 20b, those made by dividing a plurality of memory chips 11 from the semiconductor wafer 12 in the group are mounted. Hence, in comparison with the case, where after dividing a single memory

chip 11 from the semiconductor wafer 12 one by one the memory module is formed by mounting with a distance between respective memory chips 1, miniaturization of components can be realized by such high density mounting. Particularly, miniaturization of the mounting area becomes the minimum due to the CSP mounting. On the basis of quality categories, dividing is performed to produce the memory module 20a or the like including memory chips 11 as many as possible and thus, the memory module 20a or the like including many memory chips can be efficiently fabricated.

The present invention is not restricted to the above described embodiment and allows various modifications of practice in a range of scope of the present invention. For example, respective memory chips 1 included the semiconductor wafer 2 according to the above described first embodiment may connect corresponding terminals each other by a wire within respective memory chips 1. For example, a power supply terminal of respective memory chip 1 receives a common supply voltage and a clock terminal receives a common operation clock signal. In the case where respective terminals receiving the same voltage or respective terminals used for inputting the same signal are connected each other in formation of respective memory chips 1 to divide four pierces or two pieces of memory chips 1 simultaneously, it is adapted to apply the common voltage to or input the common signal in any one of four pierces or two pieces of memory chips 1. In this manner, by wiring between each other inside respective memory chips 1, the number of wires between a plurality of memory chips 1 and the substrate

4, on which these chips are mounted, can be reduced to simplify mounting procedure.

However, how to make a combination adjacent respective memory chips 1 to divide can be known until practice of quality test and therefore, as shown in FIG. 6, it is preferable to wire same terminals of all the adjacent memory chips 1 each other. In addition, the case, where the power supply terminals or the clock terminals are connected each other, has been described as an example. However, other terminals, for example, address terminals or data terminals may be connected each other. When same address terminals are connected each other, if a bit structure of one memory chip 1, for example, is 16 M × 4 bits, in the memory module 10b made by dividing simultaneously two memory chips 1, the bit structure of 16 M × 8 bits can be easily realized by using fewer numbers of the wire. In the memory module 10a made by dividing simultaneously four memory chips 1, the bit structure of 16 M × 16 bits can be easily realized by using fewer numbers of the wire. On the other hand, when same data terminals are connected each other, if a bit structure of one memory chip 1, for example, is 16 M × 4 bits, in the memory module 10b made by dividing simultaneously two memory chips 1, the bit structure of 32 M × 4 bits can be easily realized by using fewer numbers of the wire. In the memory module 10a made by dividing simultaneously four memory chips 1, the bit structure of 64 M × 4 bits can be easily realized by using fewer numbers of the wire.

Similarly, corresponding terminals of memory chips 11 contained in the semiconductor wafer 12 according to the above described second embodiment may be connected each other by wiring. However, in this case, other than the case where, in the semiconductor wafer 12 terminals of respective memory chips 11 are connected each other, it may be adapted to connect terminals of respective memory chips 11 each other by using the wire (the wiring pattern 13 shown in FIG. 5) formed in CSP mounting.

The bit configuration of respective the memory chip 1 is assumed 16 M × 4 bits in the embodiment described above, other bit configuration is possible. Besides, a combination of different bit configurations or memory chips 1 with different capacities is possible. In the embodiment described above, the case described is of an example in that the memory chip is used for the semiconductor chip to manufacture the memory module as the semiconductor device. This example can be applied to the case where the semiconductor chip of various chips other than the memory chip, for example, a processor chip and ASIC, is used for manufacturing the semiconductor device.

In the above described first embodiment, the memory module 10 is formed by mounting a plurality of or one memory chip 1, which is made by dividing, on the substrate 4. However, it may be adapted to directly mount the memory chip 1 on a mother board of a personal computer.

Industrial Applicability

As described above, according to the present invention, the unit of one or a plurality of semiconductor chips is divided from the semiconductor wafer according to the result of quality test. Therefore, when the semiconductor device, which comprises a plurality of semiconductor chips and is capable of high density mounting, is fabricated, the following accident does not occur: the whole of the semiconductor device becomes defective caused by defect of a part of semiconductor chips among them and thus, defect ratio can be reduced in fabricating the semiconductor device. Furthermore, the semiconductor device comprising a plurality of semiconductor chips can be used in a post-step and therefore, in comparison with the case where a plurality of semiconductor devices comprising a single semiconductor chip, the post-step can be simplified.

CLAIMS

1. A semiconductor device, wherein said semiconductor device is formed, after a plurality of identical semiconductor chips that are formed on a semiconductor wafer, by dividing the semiconductor chips in a unit of one or a plurality according to a result of a quality test for each semiconductor chips.

2. The semiconductor device according to claim 1, wherein said semiconductor chips are memory chips.

3. A semiconductor device, wherein said semiconductor device is formed, after wiring, resin sealing, and terminal formation are carried out for a plurality of identical semiconductor chips, by dividing the semiconductor chips in a unit of one or a plurality according to a result of a quality test or each semiconductor chips.

4. The semiconductor device according to claim 3, wherein said semiconductor chips are memory chips.

5. A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor chips on a semiconductor wafer;

a second step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; and

a third step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test.

6. The method for manufacturing the semiconductor device according to claim 5, wherein said semiconductor chips are memory chips.

7. The method for manufacturing the semiconductor device according to claim 5, wherein said plurality of semiconductor chips are divided in every group made of four pieces if four pieces are possible to handle, every two pieces if four pieces are impossible but two are possible to handle, and every one piece if two are impossible to handle, after said quality test is carried out.

8. A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor chips on a semiconductor wafer;

a second step of carrying out wiring, resin sealing, terminal formation for a plurality of said semiconductor chips formed on said semiconductor wafer;

a third step of carrying out a quality test of each of a plurality of said semiconductor chips, which is formed on said semiconductor wafer, by using said terminal formed by said second step; and

a fourth step of dividing one or a plurality of said semiconductor chips on the basis of a result of said quality test.

9. The method for manufacturing the semiconductor device according to claim 8, wherein said semiconductor chips are memory chips.

10. The method for manufacturing the semiconductor device according to claim 8, wherein said plurality of semiconductor chips are divided in every group made of four pieces if four pieces are possible to handle, every two pieces if four pieces are impossible but two are possible to handle, and every one piece if two are impossible to handle, after said quality test is carried out.

Abstract

A semiconductor device and a method for manufacturing the semiconductor device mountable with high density, which includes a simplified process but is capable of reducing a defect rate. A plurality of identical memory chips are formed on a semiconductor wafer, and a go/no-go test is conducted on all the memory chips. The semiconductor wafer is cut and divided into pieces that each consists of one, or two, or four good memory chips, and they are mounted on a substrate to form a memory module.

FIG. 1A

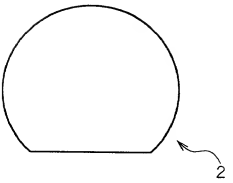


FIG. 1B

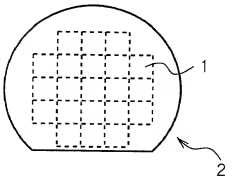


FIG. 1C

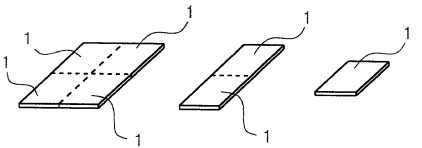


FIG. 1D

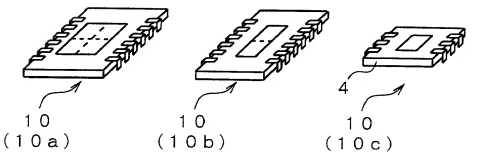


FIG. 2

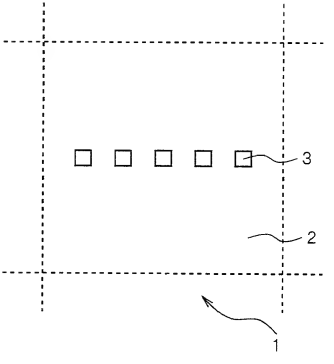


FIG. 3A

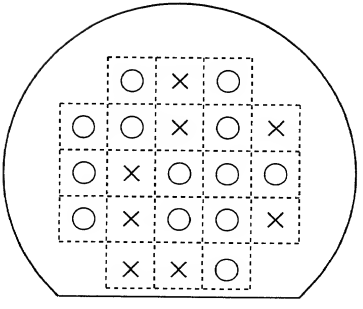


FIG. 3B

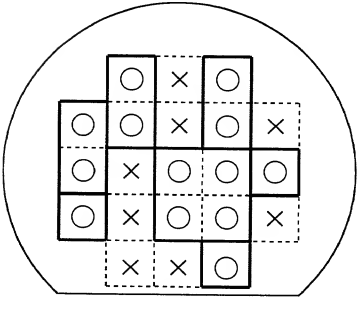


FIG. 4A

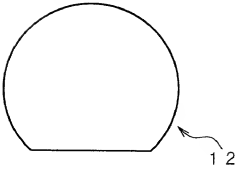


FIG. 4B

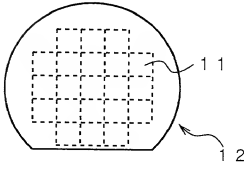


FIG. 4C

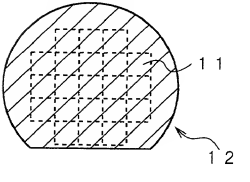


FIG. 4D

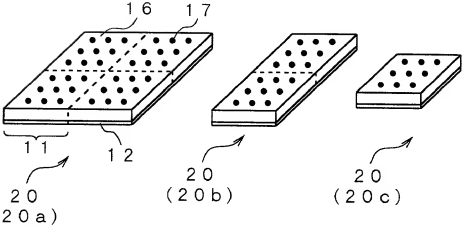


FIG. 5

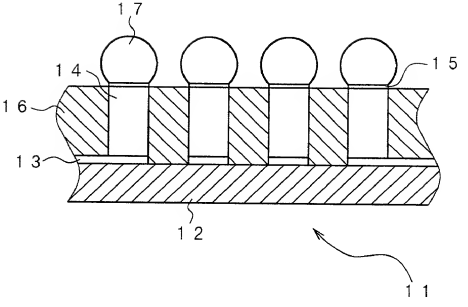
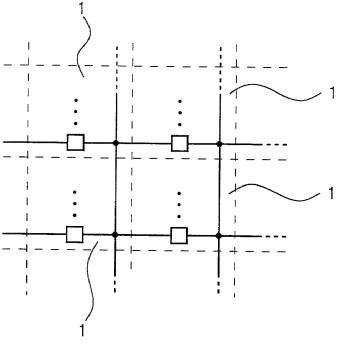


FIG. 6



Docket No.
A-382

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on **May 18, 1999** as United States Application No. or PCT International Application Number **PCT/JP99/02564**

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
10-153818	**JAPAN**	**19 May 1998**	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James H. Walters, Reg. No. 35,731

I authorize the attorney that I have appointed to accept instructions regarding this application and the resulting patent from Amagai Patent Firm.

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